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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,034	12/04/2001	Nobuharu Kobayashi	ASAM.0032	9304

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EXAMINER	
DINH, NGOC V	
ART UNIT	**PAPER NUMBER**
2187	9

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,034	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *12,14-15,17- 18* is/are allowed.

6)☐ Claim(s) *1,6,13 and 16* is/are rejected.

7)☐ Claim(s) *2-5, 7-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

FINAL REJECTION

1. This Office Action is responsive to Amendment filed 01/28/04 in which claims 6, 12, 14, 17-18 are amended.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office Action.
3. Claims 1, 6, 13 and 16 are rejected under 35 U.S.C 102(b) as being anticipated by Miyamoto et al PN 6,429,719. Claims 2- 5, 7-11 are objected. Claims 12, 14-15, 17-18 are allowed.
4. The rejections of claims 1, 6, 13 and 16 are respectfully maintained and incorporated by reference as set forth in the last office action.
5. Applicant's arguments have been fully considered but are not persuasive.
6. In the remarks, applicants argue in substance that the semiconductor disclosed by Miyamoto cannot be used in a microcomputer with the purpose of storing and comparing the identification data of the device. The comparator and implicitly the function of comparing the data in Miyamoto's semiconductor device are not disclosed.
7. The Examiner respectfully submits that applicant's position is misplaced. Mayamoto teaches a semiconductor for storing and comparing the identification data of the device [CMT, compare match time, fig. 7; col. 12, lines 5-30]. The function of comparing the identification data of the device in Miyamoto's semiconductor performed by the comparators is clearly disclosed [compare match, col. 12, line 20-25].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6, 13 and 16 are rejected under 35 U.S.C.102 (e) as being anticipated by Miyamoto et al PN 6,429,719.

8. As per claims 1:

Miyamoto teaches a semiconductor device [fig. 1, 2-4, 7] comprising: a first input/output interface circuit [SCI, fig. 7] adapted to a serial bus; an internal circuit [DMAC, fig. 7] for performing a circuit operation corresponding to a signal which is inputted or outputted through said first input/output interface circuit between said internal circuit and said serial bus; a non-volatile storage circuit [Flash, fig. 7] for storing identification data [e.g., transfer-source/destination address, col. 10, lines 30-36]; a comparator circuit [CMT, fig. 7; col. 12, lines 1-20] for comparing internal identification data stored in said non-volatile storage circuit with external identification data included in an input signal supplied through said serial bus; and a control circuit [DTC, fig. 7; col. 10, lines 1-35] responsive to an input signal subsequently supplied through said serial bus when said comparator circuit generates a match detecting signal for performing a circuit operation corresponding to said input signal; circuit operation performed by said control circuit includes: an operation for re-writing identification data into said non-volatile storage circuit in response to said input signal; and an operation directed to said internal circuit in response to said input signal [fig. 7-8; col. 9, lines 13-65; col. 11, line 53 to col. 12, line 30; col. 37, lines 5-65].

9. As per claim 6:

Miyamoto further teaches circuit operation performed by control circuit includes: an operation for re-writing identification data [e.g., read modify write, col. 18, lines 35-40] into said non-volatile storage circuit in response to said input signal; and an operation directed to said internal circuit in response to said input signal [read, write, refresh operation, col. 18, lines 30-60].

10. As per claims 13, 16:

With respect to claims 13 and 16, Miyamoto teaches a data processing system [fig. 1] comprising a plurality of semiconductor devices [fig. 2; col. 8, lines 27-35], each semiconductor device comprising: an input/output interface circuit adapted to a serial bus; an internal circuit for performing a circuit operation corresponding to a signal inputted or

outputted through said input/output interface circuit between said internal circuit and said serial bus; and a non-volatile storage circuit for storing identification data, wherein the circuit operation performed by said internal circuit includes an operation for changing said identification data [e.g., read modify write] by an input signal supplied [e.g., RAS at low level/high level] through said serial bus when an internal state transitions to a first state [fig. 7-8; col. 9, lines 13-65; col. 11, line 53 to col. 12, line 30; col. 37, lines 5-65; col. 17, line 20-67; col. 18, lines 1-44].

Allowable Subject Matter

11. Claims 2- 5, 7-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12, 14-15, 17-18 are allowed over the prior art of record.

CONCLUSION

12. THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NGOC DINH
Patent Examiner
Art Unit 2187
April 02, 2004

DONALD SPARKS
Supervisory Patent Examiner
Technology Center 2100